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PG Semester III

Paper - CC12

Unit - 4

Topic - R-2R ladder D/A converter

(ii) R-2R Ladder Type:

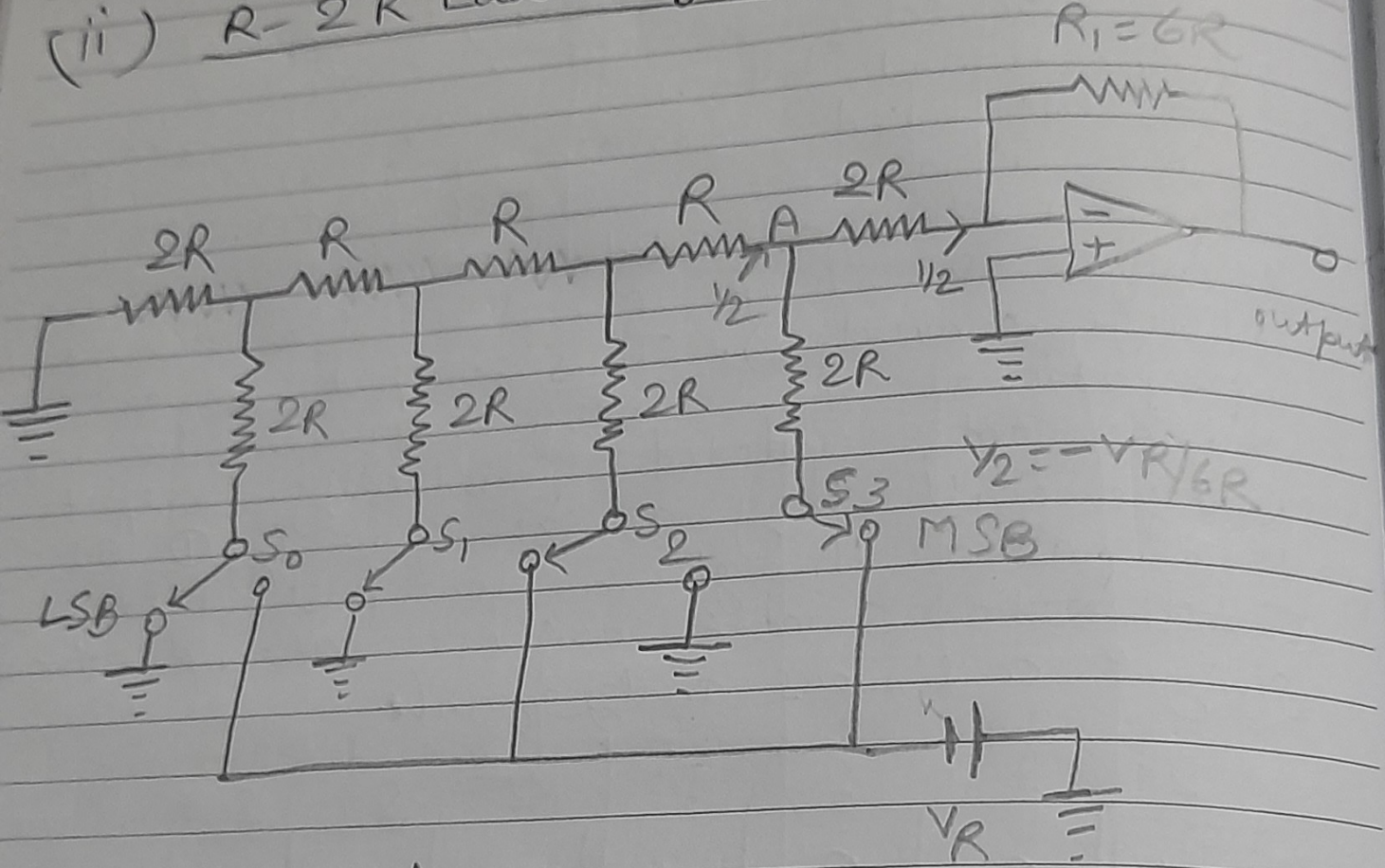

fig 1. Ladder type D/A converter.

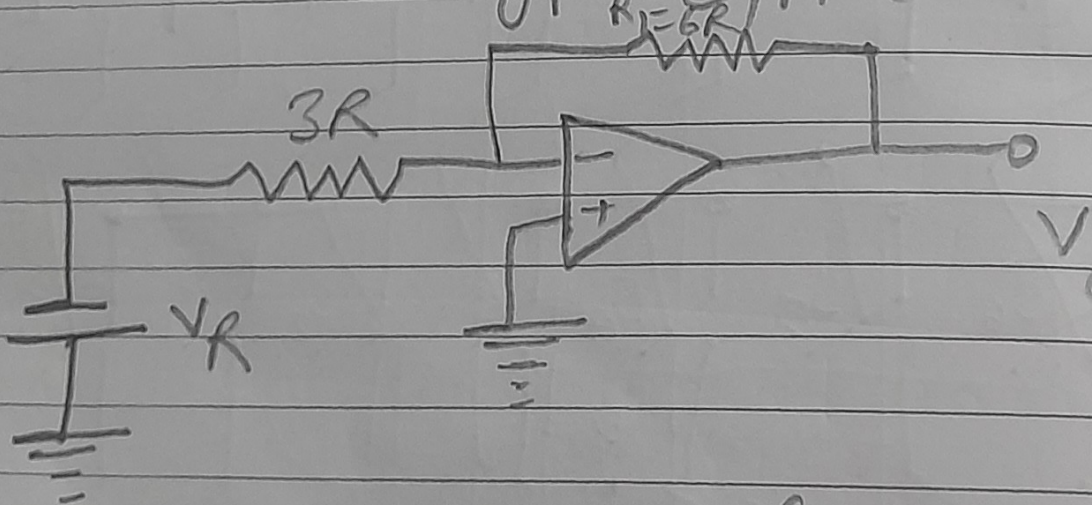

fig 2. Circuit for MSB = 1
(on using Thevenin Conversion)

In above weighted resistor type, we require various value resistors. As the number of bits increases, the ratio of the largest to the smallest resistor goes upto an unconveniently high value, making it difficult to maintain the precision. Errors also creep in due to their temperature dependance. Ladder type overcomes the difficulty by having only two values R and 2R of resistors.

Like weighted resistor type, in it two each bit of binary (held in a resistor) is associated with a switch. As shown in fig ①. if MSB is a 1, swich S_3 will connect V_R and the current I flowing into the node A will split into two equal parts at anode A.

$\frac{I}{2}$ current will flow to the left and $\frac{I}{2}$ to the right. It is because the resistance looking to the right of node A as well as to the left are equal to 2R (apply Thevenin conversion). Circuit for MSB=1 is shown in fig ②. output of OP-AMP for four stages is given by

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$$V_0 = -\frac{R_f V_R}{3R}\left(\frac{S_3}{2^1} + \frac{S_2}{2^2} + \frac{S_1}{2^3} + \frac{S_0}{2^4}\right)$$

So that for MSB,

$$V_0 = -\frac{R_f V_R}{3R}\left(\frac{S_3}{2}\right) = -\frac{6R \cdot V_R}{3R} \cdot \frac{1}{2}$$

$$= -V_R \text{ (if } R_f = 6R) \text{ or gain } \left|\frac{V_R}{V_0}\right| = 1.$$

That is, magnitude of gain from V_R to output is unity for MSB. For lower significant bits, current reaching the input of OP-AMP, as a result of successive division reduces so that gain for n^{th} bit becomes 2^{-n}.

✡ ANALOG To Digital Converter (A/D converter) Counter method

Here a counter is allowed to count clock pulses for a duration that is proportional to the amplitude of the analog sample. Thus amplitude of analog sample is quantised in terms of countings of a counter - a digital output. The duration of count is related linearly to the sample

amplitude through a gate, a comparator and an integrator fig (3)

First counter is cleared by applying a reset pulse, and switch, S, across capacitor, C, is momentarily closed and then opened thereby resetting the integrator to zero. Now integrator output rises linearly with time (ramp) but as long as it is less than sample amplitude, comparator output is HIGH and therefore allows the clock pulses to go through the AND gate to the counter which counts them. But soon as the integrator output (ramp) becomes greater than sample amplitude, the comparator becomes LOW and the gate is disabled. The counter then stops counting. Thus count accumulated in the counter is linearly related to gate duration, which in its turn is proportional to the sample amplitude. In otherwords, counter reading is the digital representation of the sample amplitude. For precision, ramp should be linear.